Service Packet

Prime Time II Digital Delay Processor

Model 95

lexicon

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1 Description

The Lexicon Prime Time II Model 95 is a versatile digital delay processor which meets the highest standards for audio delay line quality, incorporating high resolution analog-to-digital converters and carefully optimized audio circuitry for clarity and wide dynamic range. The Model 95 features up to 960 ms of audio delay (at 16 kHz bandwidth), expandable to 3.84 seconds with optional memory expansion kits. A two-stage limiter circuit prevents transient overloads, allowing greater optimization of signal-to-noise ratio.

Two independently adjustable delay outputs (each with digital display and separate mixing and recirculation controls) can be routed individually or combined in a virtually endless number of ways to create a vast array of spatial enhancements, subtle shadings, and special effects, including chorusing, double tracking, echoes, flanging, pitch twisting, resonance, vibrato, and more.

For a comprehensive description of the Model 95, refer to the Lexicon Model 95 Owner's Manual, part # 070-02991.

2 Specifications

The following specifications are subject to change without notice.

Test Conditions

Unless otherwise stated, all audio measurements are taken using a 1-kHz, 0-dBV (1 VRMS) signal source with the input and output levels referenced to the following settings: +20 dB GAIN and LIMITER switches "out," MAIN slider in the INPUT MIX section raised to the point where the +12 dB LEVEL LED lights (just before onset of A/D converter clipping as monitored from the DELAY-A OUTPUT jack), all other INPUT MIX sliders lowered to minimum, and the DELAY-A or DELAY-B slider in the OUTPUT MIX section raised to maximum, with the MASTER slider adjusted to obtain +12 dBV into 600 ohms at the MASTER OUTPUT.

Unless otherwise stated, all measurements are taken with the unit operating at room temperature.

Unless otherwise stated, all audio measurements are taken with the unit operating in XTAL mode at 16-kHz bandwidth with DEPTH control set to "0," BYPASS off, and all PHASE INVERT switches off.

Total Distortion and Noise @ 1 kHz

- 0.03% typical, 0.05% maximum.
- 0.3% maximum @ -30 dB.
- 0.1% maximum, 20 Hz to 10 kHz.

Frequency Response

- Measured with input level 12 dB below input reference level.
- 1X mode: 20 Hz to 16 kHz, +0.5, -2 dB.
- 2X mode: 20 Hz to 8 kHz, +0.5, -3 dB, referenced to 1 kHz.

Dynamic Range

- 90 dB typical, 86 dB minimum, 20-Hz to 20-kHz noise bandwidth in XTAL or VCO clock mode.

Delay Capacity

Memory Option	VCO @ 0.5X		VCO @ 1X or XTAL		VCO @ 1.5X	
	1X	**2X**	**1X**	**2X**	**1X**	**2X**
Standard	320ms	640ms	640 ms	1.28s	960ms	1.92s
Option 1	640ms	1.28s	1.28s	2.56s	1.92s	3.84s
Option 2	1.28s	2.56s	2.56s	5.12s	3.84s	7.68s

Delay Selection

- Two delay ranges are available: X1 (16 kHz bandwidth) and X2 (8 kHz bandwidth). Two individual rotary controls, each with 128 selectable delay values can select two independent delay taps. Both delays can be continuously varied over a 3 to 1 range using the MANUAL SWEEP or DEPTH controls.

Delay Step Size

- Approximately exponential, with fine adjustment available at small delay settings, with larger increments as delay is increased.

VCO Modulation

- Adjustable from none to 3:1 sweep of delay time; continuous/adjustment (blend) is available between sine wave/square wave and envelope follower functions, or external modulation. Oscillator (LFO) rate is adjustable from 0.05 Hz (20 seconds for full sweep) to 20 Hz.

Inputs

- Balanced differential inputs; MAIN INPUT is XLR-3 female connector, AUXILIARY INPUT is 1/4" tip-ring-sleeve phone jack, with 50 dB minimum common-mode rejection. Unbalanced inputs are also accepted.

Input Impedance

- Greater than 50 kilohm in parallel with 300 pF for MAIN INPUT, balanced or unbalanced.
- Greater than 20 kilohm in parallel with 150 pF for AUX INPUT balanced or unbalanced.

Input Level

- Main Input, +20 dB GAIN switch out: 0 to +19 dBV.
- Main Input, +20 dB GAIN switch in: -20 to 0 dBV.
- Aux Input: 0 to +19 dBV.

Input Limiting

- A dual slope limiter activated via a rear-panel switch allows approximately 20 dB of additional headroom without harsh clipping of input sources. Between the preamplifier and anti-aliasing filter is a compression stage with a threshold at 4 dB below reference level and a compression ratio of 4:1. Between the filter and the sample-and-hold circuit is a limiter with threshold 1 dB below reference level and a composite compression ratio of 18:1.

Outputs

- The MASTER OUTPUT is a balanced source into an XLR-3 male connector. INPUT MIX OUTPUT, DELAY-A OUTPUT, and DELAY-B OUTPUT are unbalanced and have standard 1/4" tip-sleeve phone jacks.

Output Impedance

- MASTER OUTPUT is 200 ohm balanced or unbalanced actual source impedance.
- INPUT MIX, DELAY-A, DELAY-B OUTPUTS are 600 ohm actual source impedance.

Output Level

- MASTER OUTPUT is +22 dBV (12.5 V rms) maximum when driving balanced loads 600 ohms or greater.
- MASTER OUTPUT is +16 dBV (6.3 V rms) maximum when driving unbalanced loads 600 ohms or greater.
- INPUT MIX is +16 dBV maximum when driving loads 2 kilohm or greater.
- DELAY-A and DELAY-B OUTPUTS are + 8.5 dBV maximum when driving loads 2 kilohm or greater.

Power

- 115 or 230 Vac ±10% (selectable) 50-60 Hz, 40 watts maximum. IEC power connector on rear of unit; 3-prong cord provided.

Protection

- Mains are fused (standard U.S. 3AG fuses). For export models, mains and secondaries are fused (European style 20 mm fuses). An RFI mains filter is installed.

Environment

- Operating: 0 to 35°C (32 to 95°F).
- Storage: -30 to 74°C (-22 to 167°F).
- Relative humidity: 95% maximum (without condensation).

Dimensions

- Standard 19" (483 mm) relay rack. 3 1/2" (89 mm) high by 13 1/2" (343 mm) deep.

Weight

- Net 10.5 lbs (4.76 kg); shipping 13.5 lbs (6.12 kg).

3 Performance Tests and Calibration Procedures

Performance tests can help you determine whether or not a particular unit is operating correctly. Always complete the performance tests before proceeding to calibration procedures.

The following equipment is required to complete the performance tests:

1. Variac
2. Digital Multimeter (DMM)
3. Low Distortion Audio Oscillator (with single-ended 600 ohm output)
4. Dual Trace 60 MHz Oscilloscope (with 1X and 10X probes)
5. THD+N Distortion Analyzer/Level Meter (with switchable 30 kHz low-pass or audio bandpass input filtering)
6. Pulse Generator
7. Frequency Counter (optional)
8. Frequency XY Plotter (optional)
9. Lexicon Foot Pedal (part #750-02432)
10. Lexicon Dual Control Footswitch (part #750-02433)
11. High Quality Music Source/Monitor System

3.1 Visual Inspection

1. Inspect the Model 95 for obvious signs of physical damage. Verify that all faders and switches operate smoothly.

2. Verify that all screws and connectors are secure.

3. Remove the top and bottom covers of unit and make the following checks:

   a) Verify the presence of a protective shield under the power switch and mains fuse.

   b) Verify that the voltage option switch (SW2) is set to the proper line voltage.

   c) Verify that all fuse values are correct according to Table 3.1.

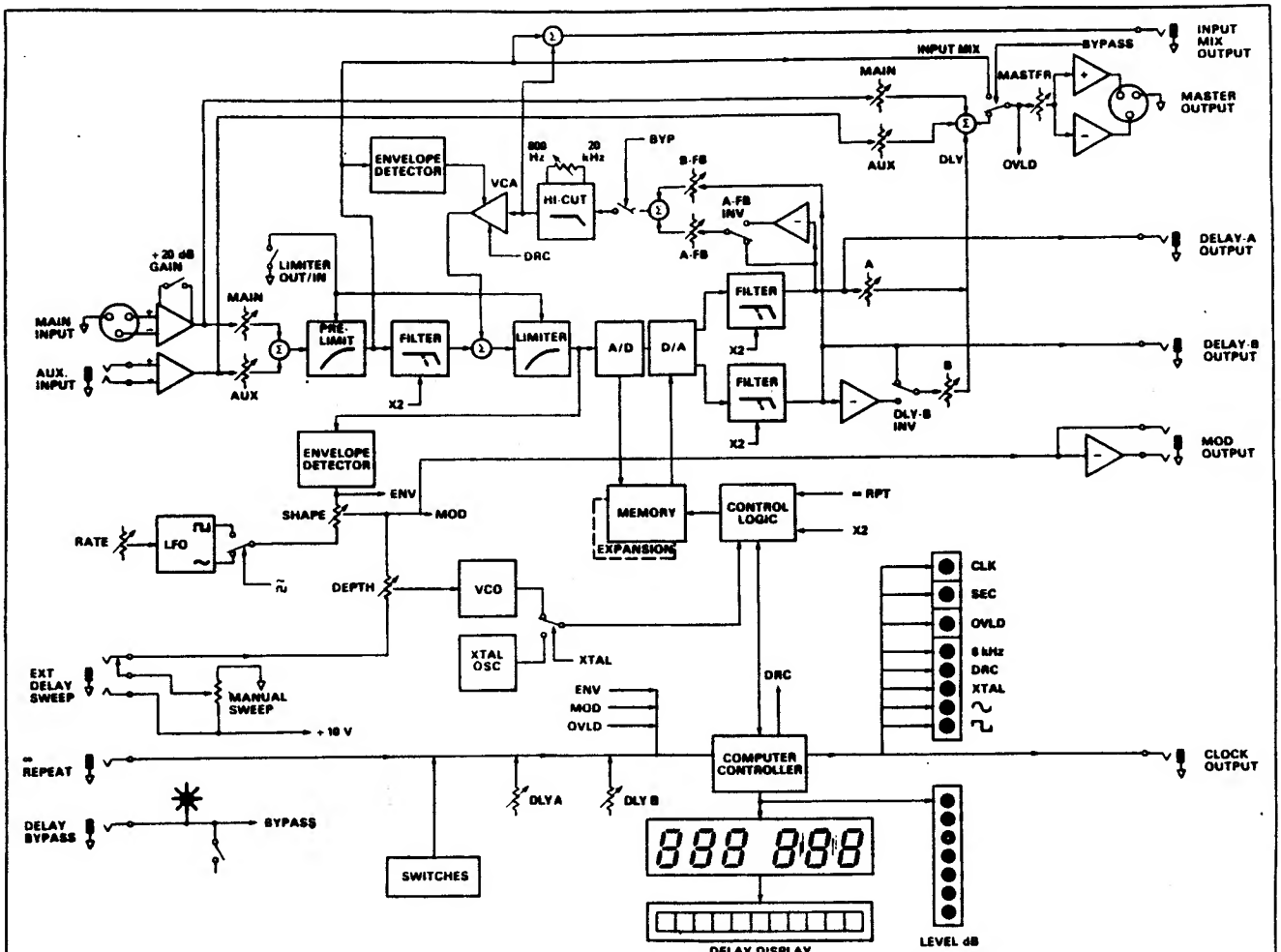


Figure 3.1. Model 95 Block Diagram

Table 3.1 Power Supply Fuses

Fuse	AC Mains Voltage		
	100V	115V	230V
F1	.750A 3AG FAST	.750A 3AG FAST	.400A 5X20mm SLO-BLO
F2	3A,250V 5X20mm SLO-BLO	----	3A,250V 5X20mm SLO-BLO
F3/F4	1.25A 5X20mm SLO-BLO	----	1.25A 5X20mm SLO-BLO

d) Verify that all socketed ICs are fully and correctly seated.

3.2 Power Supplies

The nominal and operating line voltages are as follows:

Nominal (Vac)	Operating (Vac)
100	90-110
115	105-125
230	210-250

1. Connect the Model 95 to a variac or isolation transformer.

2. Push the Model 95 POWER pushbutton on and slowly bring up the variac to the required line voltage. The current should not exceed .35 A for a 100/115 V unit or .17 A for a 230 V unit. If the unit draws excessive current, turn it off and check the supply rails for shorts.

3. Attach the common (ground) probe from the DMM to a Model 95 ground (⏚, pin 1 of P3). Measure all power supplies. Compare voltages to Table 3.2 below. All power supplies should be providing the correct voltage; if they are not, repair and/or calibration is needed.

Table 3.2. Power Supply Voltages

Supply (Vdc)	Limits (Vdc)	Location on motherboard
+5V,DIG	+4.8 V to +5.2 V	U1, pin 3
+15V	+14.4 V to +15.6 V	U2, pin 3
-15V	-14.4 V to -15.6 V	U3, pin 3
+8V,UNREG	+8.0 V to +10.0 V	P1- pin 1
+5V,ANA	+4.6 to +5.4 V	U86, pin 1
+10V,REF	Adj. R70 for 10V (±.05V)	U71, pin 3

4. For a 115 V unit reduce the variac output voltage to 100 Vac and check that all regulated voltages (+5V DIG, +15V, -15V, +5V ANA, and +10 REF) remain within their tolerance range. Return variac to 115 V.

3.3 Front Panel Test

1. Turn the Model 95 off and then on again from its front panel pushbutton. All LEDs except BYPASS should initially turn on while the main display indicates ".9.5. X.-Y." where;

   X = software version number
   Y = installed memory option (0,1,2)

   Available Memory Options

   0 = Std. Mem. -- 1.92 s maximum delay
   1 = Mem. Opt. 1 -- 3.84 s maximum delay
   2 = Mem. Opt. 2 -- 7.68 s maximum delay

2. Following the LED test, the Model 95 should initialize itself in the following mode:

   XTAL and SINEWAVE LEDs on. CLK, 8 kHz, DRC, SQUAREWAVE, and VCO MOD LEDs off.

3. Verify that the full (1X) and (2X) range of the DELAY-A and DELAY-B display corresponds to the loaded memory option. See Table 3.3 below.

   Table 3.3. Delay Capacity

Memory	VCO @ 0.5X		VCO @ 1X or XTAL		VCO @ 1.5X	
Option	1X	2X	1X	2X	1X	2X
Standard	320ms	640ms	640ms	1.28s	960ms	1.92s
Option 1	640ms	1.28s	1.28s	2.56s	1.92s	3.84s
Option 2	1.28s	2.56s	2.56s	5.12s	3.84s	7.68s

4. Activate the INF RPT function. Verify that the display alternates between delay settings and "HO LD".

5. Verify that alternate presses of the DRC switch toggle its respective LED on and off.

6. Verify that pressing the SINE/SQUAREWAVE switch alternately toggles on the indicator LEDs for these respective functions.

7. Set the DEPTH control to minimum. Verify that pressing the XTAL switch turns the XTAL LED off and the flying spot on.

8. Turn the DEPTH control to maximum. Verify that adjusting the RATE control varies the sweep rate of the flying spot.

9. Go into the CLOCK display mode. Verify that the display initially indicates "CL_OFF" followed by "01_01". Activate the CLOCK function. Note that the CLK LED flashes while mode is active.

3.4 Signal Test

Note: Use an oscilloscope and level meter to monitor the signals called out in this section. Leave all controls in their last defined position unless otherwise directed.

1. Preset the Model 95 as follows: 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS on; MAIN INPUT GAIN 0dB; LIMITER out. Set DELAY-A and DELAY-B to "00.1" ms. Lower all sliders to minimum.

2. Apply 0 dBV at 1 kHz to J12 (the MAIN INPUT jack) and J11 (the AUX INPUT jack).

3. Raise the MAIN INPUT slider to maximum. Verify that the +12 dB headroom level LED is on.

4. Decrease the oscillator level by 20 dB. Verify that the -12 dB LED is the highest headroom LED on. Push the rear panel +20 dB GAIN switch in. Verify that the +12 dB headroom LED turns on again. Return rear panel GAIN switch to its 0 dB position.

5. Lower the MAIN INPUT slider to minimum and raise the AUX INPUT slider to maximum. Verify that the +12 dB headroom level LED is again on.

6. Check J10 (the INPUT MIX OUTPUT jack) for a +12 dBV ($\pm$0.5 dB) output under no load or +6 dBV $\pm$0.5 dB output into 600 ohms.

7. Raise the MASTER OUTPUT slider for a +12 dBV output into 600 ohms from J7 (the MASTER OUTPUT jack). Refrain from readjusting this slider for remainder of section.

8. Turn off the BYPASS switch. Raise the MAIN SOURCE slider in the OUTPUT MIX section to maximum. Verify that a +12 dBV ($\pm$0.5 dB) signal level is produced at the MASTER OUTPUT jack. Lower the slider to minimum.

9. Raise the AUX SOURCE slider in the OUTPUT MIX section to maximum. Verify that a +12 dBV ($\pm$0.5 dB) signal level is produced at the MASTER OUTPUT jack. Lower the slider to minimum.

10. Raise both SOURCE sliders in the OUTPUT MIX section equally for a +12 dBV output. Activate the MAIN PHASE INVERT switch. Verify that the MAIN OUTPUT signal decreases, indicating cancellation. Return switch to its normal position and lower both SOURCE sliders to minimum.

11. Raise the DELAY-A slider to maximum. Verify that a +12 dBV ($\pm$1.0 dB) signal level is produced at the MASTER OUTPUT jack. Lower the slider to minimum.

12. Raise the DELAY-B slider to maximum. Verify that a +12 dBV (±1.0 dB) signal level is produced at the MASTER OUTPUT jack. Lower the slider to minimum.

13. Raise both DELAY sliders equally for a +12 dBV output. Activate the DELAY-B PHASE INVERT switch. Verify that the MAIN OUTPUT signal decreases, indicating cancellation. Return the switch to its normal position and lower both DELAY sliders to minimum.

14. Raise the AUX SOURCE, DELAY A and B sliders in the OUTPUT MIX section to maximum. Verify that the OVLD LED turns on at an input level of -2 dBV (±1.0 dB) for 1 kHz. Lower all the sliders in the OUTPUT MIX section (except the MASTER OUTPUT) to minimum.

15. Readjust oscillator for a 0 dBV output level at 1 kHz. Check J9 (the DELAY-A OUTPUT jack) and J8 (the DELAY-B OUTPUT jack) for a +12 dBV (±1.0 dB) output under no load or +6 dBV (±1.0 dB) output into 600 ohms.

16. Turn the DELAY-A and DELAY-B delay select controls full up. Activate the INF RPT function with a full level signal in memory. Lower the AUX INPUT slider to minimum. (MAIN INPUT slider should also be fully off.) Verify that the signal level from both the DELAY-A and DELAY-B OUTPUTS remains unchanged.

17. Repeat the last step using the rear panel INF RPT jack with an appropriate momentary closure switch, such as the one available in the Lexicon Dual Control Footswitch. Leave the Model 95 in the INF RPT mode.

18. Raise the ROLLOFF slider in the INPUT MIX section to maximum. Check the INPUT MIX OUTPUT jack for signal. At this point none should be present. Alternately raise the A-FB and B-FB RECIRCULATION sliders to maximum. Verify that each produces a +12 dBV (±1.0 dB) output under no load or +6 dBV (±1.0 dB) output into 600 ohms from INPUT MIX OUT.

19. Raise both RECIRCULATION sliders to maximum. Verify a combined minimum output from INPUT MIX OUT of +16 dBV under no load or +10 dBV into 600 ohms. (Note: A and B DELAY times must be the same.)

20. Activate BYPASS mode from rear panel DELAY BYPASS jack with an appropriate SPST latching switch; such as the one available in the Lexicon Dual Control Footswitch. Verify that the signal from INPUT MIX OUT disappears.

21. Deactivate the DELAY BYPASS function. Signal should reappear from INPUT MIX OUT. Activate the A-FB PHASE INVERT switch. Verify that the INPUT MIX OUT signal decreases, indicating cancellation. Return switch to its normal position.

22. Decrease the ROLLOFF slider to minimum. The 1 kHz signal should drop 4 dB (±1 dB). Lower both RECIRCULATION sliders to minimum and deactivate the INF RPT function.

23. Using a swept frequency XY plotter or discreet oscillator and level meter, check the frequency response of the Model 95 from its MAIN INPUT to MAIN OUTPUT through both the A and B delay taps. Set both delay taps to "00.1" (1X) mode and adjust the 1 kHz input level so that the 0 dB headroom LED just turns off. Response should be within +0.5, -2 dB from 20 Hz to 16 kHz for each delay tap. (Be sure BYPASS mode is off.)

24. Check the frequency response of the Model 95 in its (2X) mode. The response should be within +0.5, -3 dB from 20 Hz to 8 kHz for both Delay-A and Delay-B.

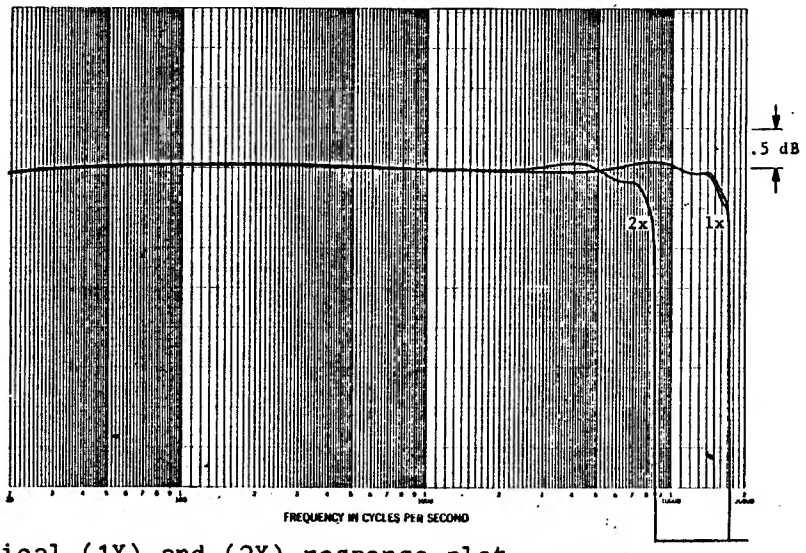


Figure 3.2. Typical (1X) and (2X) response plot.

3.5 Common Mode Rejection Test

1. Preset the Model 95 similarly to step 1 of the Signal Test section.

2. Apply 0 dBV at 1 kHz to the MAIN INPUT jack. Raise the MAIN INPUT slider to maximum. Adjust the MASTER OUTPUT slider for a +12 dBV output into 600 ohms.

3. Reconnect input signal, from unbalanced source, to both the (+) and (-) inputs (pins 2 and 3) of the MAIN INPUT jack. Verify the Model 95's output signal level is now <-50 dBV.

4. Apply 0 dBV at 10 kHz to the MAIN INPUT jack. Verify the Model 95's output signal level is <-40 dBV.

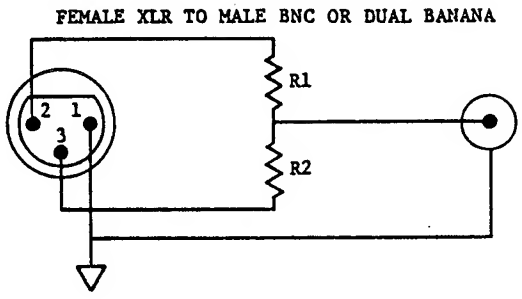
5. Repeat steps 3 and 4 for the +20 dB setting of the rear panel MAIN INPUT GAIN switch.

   Note: Lower the oscillator output by 20 dB prior to making measurement to avoid clipping the Model 95's front end.

6. Repeat steps 2 to 5 for the AUX INPUT.

3.6 Balanced Output Symmetry Test and Calibration

This test and calibration procedure requires the following special test cable to be made.



Note: R1 and R2 must be precisely matched and >20 kilohms.

Balanced Output Symmetry Test

1. Preset the Model 95 as follows: 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS off; MAIN INPUT GAIN 0 dB; LIMITER out. Set DELAY-A and DELAY-B to "00.1" ms. Lower all sliders to minimum.

2. Connect the special test cable from the MASTER OUTPUT jack to the input of the distortion analyzer/level meter. Terminate analyzer input with 600 ohms.

   Optional: If a dual trace scope is available, set both channels to .5V/DIV and the sweep time to .2ms/DIV. Connect a (10X) probe to the right sides of R55 and R56 respectively. Reference the 0V displacement of each trace to the center horizontal graticule of the oscilloscope screen.

3. Apply 0 dBV at 1 kHz to the MAIN INPUT jack. Adjust the MAIN INPUT slider for maximum converter level. This is the point where the +12 dB headroom LED just turns on.

4. Raise the MAIN SOURCE and the DELAY-A and DELAY-B sliders in the OUTPUT MIX section to the point where the OVLD LED just turns on.

5. Raise the MASTER OUTPUT slider to maximum. Note that neither polarity of the output signal display on the scope is clipped.

6. Verify that the differential output signal from the MASTER OUTPUT is <-50 dBV.

7. Switch the oscillator frequency to 10 kHz. Verify that the differential output signal from the MASTER OUTPUT is <-40 dBV.

   Note: If any of the above differential output levels are out of spec, perform the Balanced Output Symmetry Calibration procedure.

Balanced Output Symmetry Calibration

1. Repeat steps 1-5 of the Balanced Output Symmetry Test.

2. Adjust R57 to meet differential null spec at 1 kHz.

3. Retest 10 kHz performance.

3.7 Clock Out Test

1. Connect an oscilloscope between the tip and ring of J2 (the CLOCK OUTPUT jack). Activate the CLOCK function and program the DIVIDE control for 16 intervals per delay period. Verify that a positive-going pulse with a 3.5 to 5.0V amplitude appears at the CLOCK OUTPUT jack.

2. Increment the MULTIPLY control one step at a time and verify that the CLOCK LED in the main display window flashes at a constant rate.

   Note: This control programs the number of pulses per interval which will be available at the CLOCK OUTPUT jack.

3. Set MULTIPLY to 16 and DIVIDE to 1. Make sure that the Model 95 is in its 1X/XTAL mode. Measure the clock period produced by each increment of the DIVIDE control. Compare your results to the data presented in Table 3.4 for the particular memory option loaded in unit under test.

Table 3.4. Clock Period (ms) @ X16

Clock Divide	Memory Option STD	1	2
1	41.0	82.0	164.0
2	20.5	41.0	82.0
4	10.2	20.5	41.0
8	5.1	10.2	20.5
16	2.5	5.1	10.2

4. Reset the DIVIDE control to 1. Place the Model 95 in its (2X) mode. Activate the INF RPT function. Verify that the "HO LD" message appears synchronously with the CLOCK LED.

5. Deactivate the CLOCK function. Operation of INF RPT should now be immediate when its button is pressed.

3.8 Delay Test

Delay verification may be performed in one of several ways. A straightforward method using a scope and pulse generator is presented below. If only a quick check of functionality is desired, a simple listening test should suffice.

Delay Measurement

This procedure requires an externally-triggerable scope with a .1 to .5 sec sweep rate and a pulse generator with a continuous and manual trigger feature. Its pulse width should be <100ms and its output between 3.5 to 5V peak.

1. Calibrate the scope to the pulse generator as follows:

   a. Put the pulse generator in continuous trigger mode and connect its output to the external trigger and one vertical input of the scope.

   b. Set the scope's vertical input gain to 1V/DIV and its horizontal time base initially to .1sec/DIV. Be sure all control verniers are in their CAL positions.

   c. Set the scope trigger circuit to NORM.

   d. Use the scope's trigger level and XY position controls to display the output of the pulse generator.

   e. Adjust the pulse generator for a 3.5 to 5 V peak output and its pulse width <100 ms. Be sure to position the beginning of each sweep on the left-most vertical graticule line of the CRT.

2. Connect the pulse generator to the MAIN INPUT of the Model 95 and the scope to its MAIN OUTPUT.

3. Set Model 95 in its 1X/XTAL mode; INF RPT off; DRC off; BYPASS off; all PHASE INVERT switches normal; and preset DELAY-A and B to "00.1"

4. Adjust the MAIN INPUT slider for a +6 dB headroom level. Raise the DELAY-A slider in the OUTPUT MIX section to maximum. Adjust the MASTER OUTPUT slider for a 3.5 to 5V peak deflection on the scope.

5. Switch the pulse generator to its manual trigger mode. This test will initiate a sweep when each pulse is delivered to the input of the Model 95. The delayed pulse time can now be accurately measured on the oscilloscope screen.

6. Using the left-most vertical graticule line as a time zero reference, verify that each 100 ms increase in delay for tap-A will move the triggered pulse display one major graticule position to the right. For best results, use a .1 sec/DIV sweep time to measure delays up to 1 sec and .5 sec/DIV sweep time to measure delays from 1 to 5 sec.

7. Verify maximum delay time in (2X) mode.

8. Repeat steps 6 and 7 for Delay-B.

3.9 VCO Test and Calibration

This test is a continuation of the procedure used to measure delay time in section 3.8.

VCO Test

1. Place the Model 95 in its 1X/XTAL mode and set both delays to 00 ms. Turn the DEPTH, SHAPE, and RATE controls fully CCW.

2. Be sure the MAIN INPUT slider is set so that pulses aren't clipped and the DELAY-B and MASTER OUTPUT sliders are high enough for a clear scope display.

3. Set the scope's time base back to .1 sec/DIV and verify that tap-B is delaying each pulse by 500 ms. (The delayed pulse should appear precisely midway across the oscilloscope screen.)

4. Switch the Model 95 into VCO mode and set the MANUAL SWEEP control to its (1X) position. (The two center LEDs of the flying spot should be on.)

   Note: The delay time displayed on the Model 95 for (1X) MANUAL SWEEP may vary as much as 2% from what it is in XTAL mode.

5. Measure Delay-B's (1X) delay time on the scope. Verify that it is within 2% of 500 ms ($\pm$10ms).

6. Turn the MANUAL SWEEP control to its (1.5X) position. The displayed delay time on the Model 95 should indicate 750 ms. Verify delay time on scope.

7. Turn the MANUAL SWEEP control to its (.5X) position. The displayed delay time on the Model 95 should indicate 250 ms. Verify delay time on scope.

8. Plug a pot, such as the Lexicon Foot Pedal, into J6 (the VCO EXTERNAL DELAY SWEEP jack) and verify that it too can vary the VCO over its entire range.

   Note: If any of the measured delay times are outside 2% of their expected values, perform the VCO calibration procedure.

VCO Calibration

1. Repeat steps 1 - 4 of the VCO test.

2. Adjust R71 and R72 to the center of their travel (9 o'clock).

3. Tune slug T2 for 500 ms, as measured on calibrated scope graticule.

4. Set the MANUAL SWEEP control fully CW (1.5X). Adjust R72 for 750 ms, as measured on calibrated scope graticule.

5. Set the MANUAL SWEEP control fully CCW (.5X). Adjust R71 for 250 ms, as measured on calibrated scope graticule.

6. Rotate the MANUAL SWEEP control to its center (1X) position. Retune slug T2 for 500 ms.

7. Repeat (1.5X) calibration by trimming R72 to 750 ms.

8. Repeat (.5X) calibration by trimming R71 to 250 ms.

9. Switch Model 95 into XTAL mode. Verify that the scope indicates a delay time of 500 ms (±5 ms).

3.10 LFO Test and Calibration

LFO Test

1. Connect scope to J5 (the VCO MOD OUTPUT jack). Switch scope's time base to 5 ms/DIV, its vertical input gain to 2 V/DIV, and its trigger mode to AUTO.

2. Set the Model 95 as follows: turn the DEPTH and SHAPE control fully ccw; select the SINEWAVE LFO modulation function; and turn the RATE control fully CW (20 Hz).

3. Verify that a 20 - 25 Hz (50 - 40 ms period) quasi-sinewave with a 0 V to 10 V amplitude is produced at J5. See Figure 3.3 below for a reference trace.

4. Switch the LFO into its SQUAREWAVE mode. Verify it has the same frequency and amplitude characteristics as the SINEWAVE. Check that it has a 50% duty cycle.

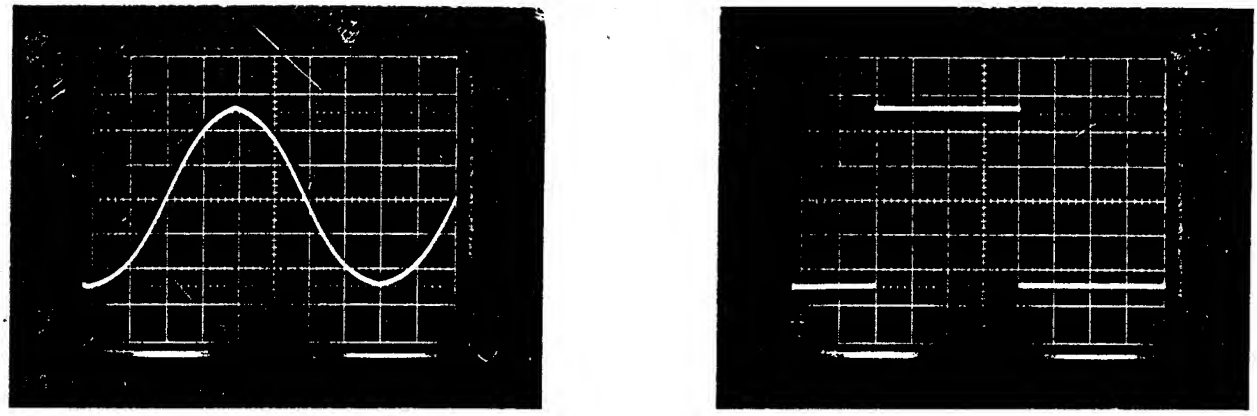


Figure 3.3 -- LFO Reference Waveforms

5. Turn the RATE control fully ccw (.05 Hz). Verify that the SQUAREWAVE's period at this rate setting is greater than 20 seconds.

6. Turn the SHAPE control fully cw (ENV). Input 0 dBV at 1 kHz to the MAIN INPUT jack. Raise the MAIN INPUT slider and verify that the MOD OUTPUT, DC signal level, varies between 0 V for no input signal and +10 V for a +12 dB headroom level.

Note: If no MOD OUTPUT signal is present at J5 or if the period/shape of the LFO waveform is incorrect, perform the LFO Calibration procedure.

LFO Calibration

1. Repeat steps 1 - 2 of the LFO Test.

2. Adjust R73 for a 20 - 25 Hz (50 - 40 ms period) quasi-sinewave LFO MOD OUTPUT waveform.

3. Parallel a 1 kilohm resistor across R109, turn the RATE control fully CCW (.05 Hz), and switch the LFO into its SQUAREWAVE mode.

4. Switch the scope's time base to 50 ms/DIV.

5. Trim R74 for a 50% duty cycle waveform.

6. Disconnect the 1 kilohm resistor across R109 and repeat steps 2 - 5 of the LFO Test.

3.11 Distortion Test and Converter Calibration

Distortion Test

1. Reset the Model 95 as follows: 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS off; MAIN INPUT GAIN 0 dB; LIMITER out. Set DELAY-A and DELAY-B to "0.001" ms. Lower all sliders to minimum.

2. Input 0 dBV at 1 kHz to the MAIN INPUT jack.

3. Adjust the MAIN INPUT slider for maximum converter level. This is the point where the +12 dB headroom LED just turns on.

4. Connect a scope and THD distortion analyzer to the Model 95's main output jack. Filter the analyzer's input with a 30 kHz low-pass or audio bandpass filter.

5. Set the MASTER OUTPUT level for +12 dBV into 600 ohms with the DELAY-A OUTPUT slider raised to maximum. Verify that distortion is <.03%.

6. Decrease the output of the oscillator 20 dB. Being careful not to alter any of the Model 95's control settings, measure distortion. It should be <.20%.

7. Increase the output of the oscillator 20 dB. Measure distortion for DELAY-A tap at its maximum (1X) and (2X) settings. In both cases, it should be <.05%.

8. Repeat steps 5 - 7 for the DELAY-B tap.

Distortion in VCO Mode

9. Return the Model 95 to its (1X) mode; set the DEPTH control fully CCW (off); turn off the XTAL; and adjust the MANUAL SWEEP control to its (1X) position. Measure distortion. It should be <.05%.

10. Turn the MANUAL SWEEP control to its (1.5X) position. Measure distortion. It should be <.10%.

11. Turn the MANUAL SWEEP control to its (.5X) position. Measure distortion. It should be <1.5%.

12. Drop the oscillator level 10 dB and switch its frequency to 10 kHz.

13. With the MANUAL SWEEP control in its (.5X) position, measure distortion. It should be <.20%.

14. Turn the MANUAL SWEEP control to its (1.5X) position. Measure distortion. It should be <1.5%.

If any of the above distortion measurements were out of spec, perform the Converter Calibration procedure below.

Converter Calibration

1. Repeat steps 1 - 5 of the Distortion Test.

2. Adjust R67 and R68 for minimum distortion.

3. Decrease oscillator level 20 dB and adjust R64 for minimum distortion. Providing there are no faulty components in system, the THD here should be <.20%.

4. Increase oscillator level 20 dB and readjust R67 and R68 for minimum distortion. THD here should be <.03%.

5. Repeat steps 7 - 14 of the Distortion Test.

Note: If distortion is still out of spec after recalibrating the converter, use standard troubleshooting techniques to isolate the exact location of the problem. Try connecting a 1X probe to the distortion analyzer and marching stage by stage through the analog circuits. If everything looks OK up to the converter but not after it, bypass the entire digital section and recheck the output. To do this, lift one side of R79 and connect a jumper from the junction of R153/R154 to either output of U73. If the problem appears to be in the converter/digital section, use a scope and (10X) probe to verify presence of all system clocks and the functioning of all chip enable signals. Look for activity on the data and address buses.

3.12 Limiter Test and Calibration

Limiter Test

1. Preset the Model 95 as follows: 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS off; MAIN INPUT GAIN 0 dB; LIMITER out. Set DELAY-A and DELAY-B to "00.1" ms. Lower all sliders to minimum.

2. Input 0 dBV at 1 kHz to both the MAIN and AUX INPUT jack. Raise the MAIN INPUT slider to where the +12 dB headroom LED just turns on.

3. Connect the distortion analyzer/level meter and scope to the INPUT MIX OUTPUT jack. Measure distortion. It should be <.01%.

4. Take note of the signal level at the INPUT MIX OUTPUT jack. It should have a +10 dBV (±0.5 dB) output under no load or +4 dBV (±0.5 dB) output into 600 ohms.

5. Engage the LIMITER. The level of the INPUT MIX OUTPUT signal should drop 2 dB (±1.5 dB).

6. Increase the oscillator's output 10 dB to +10 dBV. The INPUT MIX OUTPUT signal should now increase 3 dB (±2 dB).

7. Raise the AUX INPUT slider to maximum. The INPUT MIX OUTPUT signal should further increase 4 dB, (±1.5 dB).

8. Measure distortion. It should be <.3%.

9. Slowly increase the oscillator's output level while viewing the THD distortion residue on the scope. Continue until spikes indicating input stage clipping appear. Back off the oscillator level until the spikes just disappear.

10. Reconnect the distortion analyzer/level meter and oscilloscope to the MAIN OUTPUT jack.

11. Set the MASTER OUTPUT slider for a +12 dBV into 600 ohms with the DELAY-A OUTPUT slider raised to maximum.

12. Measure distortion. It should be <1.0%.

13. Lower the AUX INPUT slider to minimum. Verify that the level of the MASTER OUTPUT doesn't drop more than 1 dB.

If any of the above level or distortion measurements were out of spec, perform the Limiter Calibration procedure described below.

Limiter Calibration

1. If limiter performance fails to meet spec by step 8 of the test procedure, try selecting another CLM50 for U84 and retest. Due to manufacturing tolerances in these devices, there is expected to be some fallout.

2. If failure to meet spec occurs at step 12, adjust R116 for minimum distortion. It should be [1.0%. Should this also fail, select another CLM50 for U108, readjust R116 and perform Limiter Test procedure again.

3.13 DRC Test and Calibration

DRC Test

1. Preset the Model 95 as follows; 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS off; MAIN INPUT GAIN 0 dB; LIMITER out. Set DELAY-A and DELAY-B to maximum. Lower all sliders to minimum.

2. Input 0 dBV at 1 kHz to the MAIN INPUT jack.

3. Adjust the MAIN INPUT slider for maximum converter level. This is the point where the +12 dB headroom LED just turns on.

4. Activate the INF RPT function.

5. Connect a distortion analyzer/level meter, via a (1X) probe, to the junction of C130 and R79 (the right side of R79). Be sure to remove the 600 ohm load terminator from the analyzer's input. Verify an in-circuit signal level of approximately +10 dBV.

6. Activate the DRC function and raise the A-FB, B-FB, and ROLLOFF sliders in the INPUT MIX section to maximum.

7. Change the oscillator frequency to 2 kHz and check distortion. It should initially measure [.5%, although it may slowly rise above this point. If the Model 95 fails to meet this spec, perform the DRC calibration procedure.

8. Switch the distortion analyzer back to measure level and lower the MAIN INPUT slider to its halfway point.

9. The in-circuit signal level should decrease by approximately 12 dB, and then rise again as the slider is lowered to minimum.

DRC Calibration

1. Repeat steps 1 - 7 of the DRC Test procedure.

2. Adjust R140 for minimum distortion. This should initially measure [.5%. If the DRC circuit fails to meet this spec, try selecting another CLM50 for U89 and retest. Due to manufacturing tolerances in these devices, there is expected to be some fallout.

3.14 Noise Test

1. Preset the Model 95 as follows: 1X/XTAL mode; INF RPT off; CLOCK off; DRC off; all PHASE INVERT switches off; BYPASS on; MAIN INPUT GAIN 0 dB; LIMITER out. Set both DELAY-A and Delay-B to "00.1" ms. Lower all sliders to minimum.

2. Connect shorting plugs to both the MAIN and AUX INPUT jacks.

3. Connect a distortion analyzer/level meter to the MASTER OUTPUT jack. Filter the input to the analyzer with a 30 kHz low-pass or audio bandpass network. Terminate its input with a 600 ohm load.

4. Raise the MASTER OUTPUT slider to maximum. Measure noise. It should be <-78 dBV.

Input Mix Section

5. Raise the MAIN INPUT slider to maximum. Measure noise. It should be <-79 dBV.

6. Raise the AUX INPUT slider to maximum. Measure noise. It should be <-78 dBV.

7. Activate the rear panel +20 dB GAIN switch. Measure noise. It should be <-75 dBV. Deactivate switch.

8. Lower the MAIN and AUX INPUT sliders to minimum, turn BYPASS off. Measure noise. It should be <-82 dBV.

9. Reconnect the distortion analyzer/level meter to the INPUT MIX OUTPUT jack. Measure noise. It should be <-82 dBV.

Output Mix Section

10. Reconnect the distortion analyzer/level meter to the MASTER OUTPUT jack.

11. Raise the MAIN SOURCE slider to maximum. Measure noise. It should be <-80 dBV.

12. Raise the AUX SOURCE slider to maximum. Measure noise. It should be <-77 dBV.

13. Lower both the MAIN and AUX SOURCE sliders to minimum. Raise the DELAY-A OUTPUT slider to maximum. Measure noise. It should be <-72 dBV.

14. Raise the DELAY-B OUTPUT slider to maximum. Measure noise. It should be <-67 dBV.

3.15 Shock and Critical Listening Test

1. Connect a high quality music source and monitor system to the Model 95.

2. Set up proper signal levels through machine.

3. Exercise each pot and slider individually. No intermittents or scratchiness should be heard.

4. Setup several effects (chorusing, long echoes, etc.) and perform critical listening tests for excess or unusual noise, birdies, or other audio irregularities.

5. Verify that the Model 95 can be powered up in maximum delay free of beeps, honks, or other evidence of memory trash.

6. Perform shock tests while listening to verify overall mechanical integrity of unit.

7. Attach top and bottom covers.

4 Circuit Description

The information contained in this section is provided as an aid to qualified service personnel. It is not intended to be a primer in analog and digital circuit theory, but rather a guide to the organization and function of the various circuit blocks within the Model 95.

4.1 Analog Circuitry

4.1.1 Audio Input

The main input signal enters the Model 95 through a female XLR connector and goes to a balanced two stage differential input buffer which converts the signal to single-ended form. Overvoltage and RFI protection is performed at the input. A rear panel pushbutton switch sets the gain of the input buffer at +20 dB (in) and 0 dB (out).

The next stage is a unity-gain summing circuit with an attenuation range (via main in and aux in slide pots) of 0 dB to (theoretically) infinity.

The summed input signal then goes to a variable gain stage. With the rear panel limiter switch in the out position, the gain of this stage is fixed at 12 dB. With the limiter switch in, the gain of this stage is 12 dB until its output reaches a level of +8 dBV, whereupon a compression ratio of 4:1 begins. When the output level of this stage reaches approximately. +14dBV, and beyond, the circuit operates at close to unity gain.

4.1.2 Input Filter, Input Envelope, Input Mix, Bypass

The audio signal is then sent to four places:

1. input filter
2. input envelope follower
3. input mix output buffer
4. bypass circuit

Input Filter

The input filter is a 7 pole elliptical low-pass filter to remove frequency components above 16.5 kHz (1X). In the 2X mode, this cutoff frequency is reduced to 8 kHz via CMOS switches which parallel additional capacitors into the filter. The filter has a gain of -6 dB ($\pm$ 0.25 dB) within its pass band.

Input Envelope Follower

The input envelope follower serves a dual purpose; it drives the input compression circuit and provides a voltage proportional to input level for the DRC circuit. It is comprised of a full-wave rectifier of unity gain followed by two different lowpass filters to provide smoothing. The first filter

provides the time constant and offset bias to properly control the input compression stage. The second provides a smoothed, level dependent voltage source for the DRC (dynamic recirculation control) drive circuit.

Input Mix Output buffer

The input mix output buffer is a single-ended unity gain driver which sums the compressed input mix signal with the recirculated signal and sends it to the Input Mix Output phone jack.

Bypass Circuit

The bypass circuit can be activated by either the front panel toggle switch or an external switch to ground via the Delay Bypass phone jack on the rear panel. It shunts the output mix to ground and accesses the input mix signal to the master output slider, and also shunts the recirculation signal to ground. This function is performed by a CMOS switch. A front panel LED lights when bypass is activated, whether by the switch or remotely. To clarify, the bypass circuit eliminates "processed" signal from the master output and the in-mix output. The Delay-A and Delay-B outputs are unaffected except that the signal can no longer be recirculated.

4.1.3 Dynamic Recirculation Control, Sum, Aperture

From the input filter the audio signal goes to a stage which provides a gain of 6 dB and sums this signal with the recirculated signal. The gain of the circuit is 0 dB for the recirculated signal, unless the DRC function is activated. With the DRC function on, the previously mentioned input envelope follower provides a smoothed, input level-dependent voltage which is then amplified and offset to drive a VCA in the aforementioned summing circuit. This circuit attenuates the recirculation signal by 3 dB at an input mix signal level of approximately -16 dBV, and goes to approximately 60 dB down at maximum input level.

The resultant summation is passed through an aperture correction circuit which provides a high frequency boost to compensate for the aperture loss inherent in the sampling process. It is a 2 pole low pass filter with a Q of 1.5 which yields approximately 2 dB of boost at the filter cutoff frequency. In 2X mode, the boost frequency is reduced to compensate for the reduced sample rate by a CMOS switch which parallels additional capacitors into the circuit.

4.1.4 Pre-limit And Pre-emphasis

Following aperture correction the analog signal enters a circuit which provides the dual function of pre-converter limiting and pre-emphasis. Pre-emphasis gives a high-frequency shelving, providing about 10 dB of boost at 16 kHz. The time constants are 12us and 50us for the pole and zero, respectively.

Limiting occurs in the following manner. The circuit has unity gain for frequencies below the zero of the pre-emphasis (about 3 kHz) until the output reaches a level of 1 dB below maximum converter level (+12 dBV). At this point, the circuit begins limiting (actually a very steep compression) with a ratio of approximately 12 to 1. This ensures that any peaks in the audio signal entering the machine will not overrange the converter--the input stages

will clip for excessive input levels before the converter will. This has the advantage of preventing harsh sounding converter clipping inherent in many other digital audio processors.

The output of the limiter circuit goes to the converter and to a precision full wave rectifier with peak hold. Peak hold is accomplished by incorporating a transistor in the emitter follower configuration charging a capacitor within the feedback loop of the operational rectifier. The maximum output voltage of this circuit is limited to approximately 4.7 V by the resistive divider at the base input to the emitter follower. This prevents overranging the A/D converter of the microprocessor, which uses this voltage to generate the headroom level indication. This peak hold circuit also drives two other circuits; the pre-limit drive and the envelope function for the VCO.

The pre-limit drive circuit is a high-gain noninverting driver with adjustable offset so that its turn on threshold can be trimmed to the proper level.

4.1.5 Digital Delay Conversion

The analog input signal is sampled at 34 to 102 kHz in the (1X) mode and 17 to 51 kHz in the (2X) mode. Following the sample and hold, the signal passes through a log amplifier circuit which compresses its dynamic range. This logarithmic compression enables the A/D converter to encode a greater dynamic range. The sample is converted into a 12 bit digital magnitude applying the successive approximation method using an SAR, D/A converter, and comparator. Timesharing of the D/A converter is required for input as well as both output audio channels. Four 12 bit latches are used to transfer parallel 6 and 12 bit data as follows:

1 - Hold two 6 bit Delay-A bytes for the D/A converter
2 - Hold two 6 bit Delay-B bytes for the D/A converter
3 - Hold 12 SAR bits for two 6 bit memory inputs
4 - Hold 12 SAR bits as zero delay for the D/A converter.

A memory address counter is constantly cycling and generating write addresses for the 6 bit wide memory. Two 6 bit bytes are taken from the holding latch (as 3 above) and written into memory locations pointed to by the address counter. The two offset registers, which contain the delay offset values, are added to the current write address counter value generating a new address which is used to point to the offset read locations. The data extracted from memory at these new addresses is placed into the holding latches (as 1 & 2 above) and represents the Delay-A and Delay-B data output channels.

As the memory counter addresses the entire memory sequentially as a write pointer, the Delay-A and Delay-B read pointers will follow the write pointer by a magnitude which is proportional to the delay offset values. Finite timing and control are generated from a faster counter ahead of the memory address counter and a ROM to provide the high/low byte transfer pulses, converter SAR clocking, and memory read/write signals. To provide the repeat function, the repeat enable flop simply prevents memory writing thereby retaining current memory contents for repetitive Delay-A and Delay-B read cycles.

Timesharing the D/A converter occurs in each word-cycle of the timing control logic as follows. During the first phase, a new analog sample is converted

using the D/A converter with the comparator and memory reads fill the Delay-A/Delay-B latches. During the second phase the D/A converter is used to convert the Delay-A/Delay-B latched output data and write the new converted sample into memory.

When memory options are installed they provide a grounding signal which causes logic to automatically enable extended memory addressing during assembly. The following chart shows the amount of memory and the amount of delay possible with each memory option.

	1X Mode			2X Mode			
OPT	.5X	1X	1.5X	.5X	1X	1.5X	MEMORIES
STD	0.32s	0.64s	0.96s	0.64s	1.28s	1.92s	6
OP1	0.64s	1.28s	1.92s	1.28s	2.56s	3.84s	12
OP2	1.28s	2.56s	3.84s	2.56s	5.12s	7.68s	24

4.1.6 Digital Outputs, De-emphasis, Output Filters

The D/A converter current output is converted to a voltage and passed onto an anti-log amplifier circuit which will re-expand the dynamic audio range to provide the inverse function of the input log circuit. A common diode array is biased to provide the log function and temperature stable characteristics. Biasing is trim adjustable to compensate for resistor and diode differences, enabling distortion correction. Having been restored, the audio signal is sampled and switched into the Delay-A and Delay-B output deglitchers. The outputs of the converter deglitchers go on to the de-emphasis networks which, as the name suggests, perform the inverse function of the pre-emphasis network. The net result is a flat band response.

From here the A & B delayed analog signals pass through their respective output filters. The output filters, like the input filter, are 7 pole elliptical low pass filters with a cutoff frequency of 16.5 kHz. In the 2X mode, additional capacitors are switched in via CMOS switch ICs which reduce the cutoff frequency to 8 kHz. Each filter (whose gain is -6dB) is followed by a noninverting buffer with a gain of 6dB.

The outputs of the A and B channel filters are routed to unity gain buffers which drive the single-ended Delay-A and Delay-B outputs. These signals are also routed to the A-FB & B-FB sliders in the input mix section and the Delay-A and Delay-B sliders in the output mix section. In the recirculation path the A and B feedback sliders are summed and the output goes to a single pole (-6 dB/octave) low pass filter with a cutoff frequency adjustable via a front panel slider from 20 kHz down to 800 Hz. The output of the filter is buffered and sent to the in-mix output driver and the VCA, where it is summed back into the input path as previously described.

In the output mix section the Delay-A and Delay-B sliders are summed at unity gain along with the Main and Aux Source sliders (at a gain of 12 dB). This output mix signal goes to the Master Output slider and to a peak hold circuit.

The peak hold uses a fullwave operational rectifier driving an emitter follower, which charges a capacitor with a high impedance discharge path resulting in a long peak storage time constant (1/3 second). The maximum

output voltage of this circuit is limited by a resistive divider at the base of the emitter follower transistor to +4.0 V. This prevents overvoltage to the A/D converter input which references to +5.0 V. The A/D converter reads this signal to determine if the output mixer is being overloaded and the CPU will signal this condition by lighting the overload LED on the front panel.

The Master Out slider is buffered and sent to a balanced transformerless output driver capable of driving a 600 ohm balanced load to +22 dBV, via a male XLR connector on the rear panel.

4.1.7 LFO (Low Frequency Oscillator)

The variable-rate LFO has both sine and square wave outputs, selectable by a CMOS switch. A very precise 10 V reference voltage is provided from the +15 V supply by an LM317 voltage regulator and all signals in the LFO are referenced to this voltage. Consequently all signals and signal mixes have a maximum swing of 0 to 10 V, preventing the VCO from producing frequencies beyond its intended range.

An operational integrator with a variable time constant, via the front panel rate potentiometer, produces a ramp which is fed to a transconductance amplifier which is in an inverting mode and is biased such that the ramp is "rounded". When the ramp (at its input) changes direction, resulting in a triangle waveform, the output of this transconductance amplifier is a very close approximation to a sine wave. This signal is routed to the CMOS waveform selection switch and to an open collector comparator with hysteresis.

This comparator converts the sine wave to a square wave with a preset swing of 0 to 10 V. This signal then goes to the CMOS switch and to an operational amplifier with a gain of two and a -5 V offset to produce a square wave of -10 to +10 V. This signal feeds the rate pot. When this signal changes state, it causes the integrator to reverse direction, starting a ramp of opposite slope. Thus a triangle wave is generated which goes back through the loop creating the sine and square wave signals. The selected waveform is then buffered and sent to the shape pot on the front panel.

The peak hold signal is read by the A/D converter and drives the pre-converter limiter previously mentioned. It is amplified for a 0 to 10 V swing, and sent to the other end of the shape pot. Turned fully ccw, the output of the shape pot will be only the selected output of the LFO. Turned fully cw, the output will be only the amplified output of the peak hold circuit. At any other setting the output will be a proportionate mixture of both signals.

The resultant signal is then routed to the depth pot and to a unity gain, noninverting, buffer whose output goes to the tip of the modulation output jack on the rear panel. This composite signal also goes to an inverting unity gain buffer with +5 V of offset creating a signal of opposite phase yet still restricted to a 0 to +10 V swing, which continues to the ring of the modulation output jack. With this output configuration it is possible for multiple units to be modulated from the same source either in phase, or 180 degrees out of phase for stereo processing.

The front panel Manual Sweep control allows manual adjustment of the VCO clock frequency by putting out a voltage between 0 and 10 V. This control can be

overridden by plugging an external pot into the External Delay Sweep jack on the rear panel. This pot should have its ends connected to the ring and sleeve, with the wiper connected to the tip of the plug. Sweep can also be controlled by an external voltage source (not to exceed 10 v) with ground connected to the sleeve and the voltage connected to the tip, with the ring left unconnected. Clamping diodes are provided to protect against overvoltage. The sweep input voltage is buffered and then sent to the other end of the depth pot. At full cw, the depth pot output is only the modulated signal coming from the shape pot. Turning the depth pot fully ccw produces only the sweep voltage. Anywhere in between produces a proportionate mix of these two signals.

4.1.8 Voltage Controlled Oscillator

The output of the depth pot goes to a unity gain inverting buffer with an offset of +5 V, resulting in a signal of opposite phase as the input, but still operating in the 0 to +10 V range of the LFO. This signal then goes to the A/D converter in the CPU section to be used to display VCO modulation on the "flying spot" display and is also routed to a VCO calibration/driver circuit. The drive circuit is calibrated to properly modulate the VCO by adjusting the voltage output at the sweep end points. With the Depth control turned fully counter-clockwise and the Manual Sweep control set at 1.5X (lowest clock frequency) the circuit puts out approximately 3.5 V. With the Manual Sweep at .5X (highest frequency), the circuit puts out approximately 12 V. The gain of this circuit compensates for the fact that for the 5 V input change from 1X to .5X the VCO frequency must double, while for the 5 V input change from 1.5X to 1X, the frequency increases only 50%.

The VCO circuit consists of an L/C tank, driven by a digital inverter. The inductor is a slug-tuned coil, which is tuned to the 1X frequency of 2.4576 mHz. Ability to vary the frequency as a function of modulation voltage is made possible by the use of back-to-back varactor diodes whose capacitance varies fairly linearly with the input bias voltage. A 1 Kilohm bias resistor provides negative feedback to the inverter ensuring that the oscillations are self-starting by biasing its input into the linear range of the device. Output from this inverter passes through a single pole low pass filter to dampen any ringing of the VCO clock signal and then through two additional inverter stages to clean up the rising and falling edges. Due to the high Q of the L-C tank, this produces a clean, stable digital clock waveform.

4.2 Digital Circuitry

4.2.1 Microprocessor Inputs

An eight channel, single ended, multiplexed input, successive approximation A/D converter is provided for panel and other analog inputs to the microprocessor. The CPU scans the A/D converter inputs, sampling and processing each individually. The scan sequence of channels 0 through 7 is indicated below:

0 Delay-A
1 Delay-B
2 VCO Modulation
3 Input Envelope
4 Overload Detector
5 Switch Group-1
6 Switch Group-2
7 Memory Size

The Delay-A and Delay-B inputs are voltages derived directly via the front panel delay selection pots. VCO Modulation is sampled from the depth control output buffer and enables the CPU to generate the "flying spot" display. Headroom level is derived from the input peak hold voltage and the overload indication level is derived from the output overload detector. Pushbutton switch inputs on the front panel are divided into two groups of three switches per group. Group one consists of repeat hold, Clock Multiples, and Clock Divisions. Group two consists of DRC, LFO waveform, and Xtal mode switches. Each switch group provides multiple voltage levels to the A/D converter generated from resistors paralleled with push buttons depressed as in a ladder network. The last input (channel 7) is a voltage level derived through a resister network which is grounded as memory options are installed indicating to the CPU the memory option level.

Two digital input signals to the CPU are used to service wait states and to interrupt the programmed scan sequence. When delay settings are changed the CPU holds up in a wait state until the request is synchronized and accepted by the delay timing logic. Whereupon the delay timing signal WC4 clears the wait state flop enabling the CPU to continue processing. The second digital input is the interrupt signal to the CPU. It is MA6 from the delay memory address timing counter which causes 1.25 ms to 3.75 ms interrupt periods. These periods are counted by the interrupt handler routine to provide the selected clock output function.

4.2.2 Microprocessor Outputs

All CPU outputs are latched. However, both the data bus and the address bus are used to provide data information. Also, both the read and write signals are used to control data outputs. No port or I/O CPU control decoding exists, instead all latches and the input A/D converter are memory mapped into the system. This simply means these latches are accessed by the system program as memory locations.

The Delay-A and Delay-B offset latches receive 14 CPU address bits as delay offset selection data. This data is in the complimented form so that when added to the current memory address counter the results will point to a location behind (less than) the current write position. Since Delay-B latch is clocked using the CPU write signal, it also stores the Zero-A and Zero-B signals from the CPU data bus. And the address bus is clocked into the Delay-A latch using the CPU read pulse.

Front panel displays are multiplexed through a shared 8 bit current source, a 6 bit digit sink, and a 5 bit LED sink. Source data is derived from the address bus and sink data from the data bus. One or more sources may be on at a time, however, only one sink bit is on at a time. In other words the source latch holds display information and the sink latches indicate which display gets the information. The remaining 5 latch bits are used to enable Feedback DRC, 2X Mode, Xtal Mode, LFO Waveform Selection, and Clock Output Signal. A discrete flop is used, via the CPU, to enable the repeat function. Timing overlay of the front panel current sources and sinks are programmed into the display scan cycle such that the sinks on/off conditions await current source settling.

5 Parts List

The following parts lists are contained in this section in the order listed:

Lexicon Model 95 Front Panel #1 Board

PART NO.	QTY	DESCRIPTION	REF.
POTENTIOMETERS			
200-02616	2	POT,RTY,PC,10K-U,1/8X3/4	R1,2
200-02999	3	POT,RTY,PC,10K-U,1/8X5/8	R4-6
200-03000	1	POT,RTY,PC,25K-A,1/8X5/8	R7
200-03006	10	POT,SLD,PC,20K-A,20MMX45MM	R8-12,26-30
CARBON FLM RES			
202-00510	1	RES,CF,5%,1/4W,51 OHM	R3
202-00527	1	RES,CF,5%,1/4W,750 OHM	R16
202-00531	1	RES,CF,5%,1/4W,1.5K OHM	R32
202-00570	1	RES,CF,5%,1/4W,100K OHM	R31
METAL FLM RES			
203-00464	5	RES,MF,1%,1/8W,4.99K OHM	R13-15,18,20
203-00475	1	RES,MF,1%,1/8W,11.5K OHM	R24
203-00482	5	RES,MF,1%,1/8W,20.0K OHM	R17,19,21-23
203-00489	1	RES,MF,1%,1/8W,71.5K OHM	R25
NETWORK RES			
205-01133	1	RES,NET,DIP,1%,10KX8	RP2
205-02900	1	RES,NET,DIP,2%,120X8	RP1
ELECTROLYT CAP			
240-00611	2	CAP,ELEC,22uF,16V,RAD	C18,19
240-00614	1	CAP,ELEC,47uF,16V,RAD	C1
PCRB/PP CAP			
244-00660	1	CAP,MYL,.01uF,100V,10%,RAD	C16
CERAMIC CAP			
245-00600	4	CAP,CER,.02uF,35V,80/20%	C3-6
245-01164	6	CAP,CER,10pF,50V,10%	C9,10,13-15,17
245-01651	5	CAP,CER,.1uF,50V,80/20%	C2,7,8,11,12
LINEAR IC			
340-01566	2	IC,LINEAR,LF353,DUAL OP AMP	U5,7
340-02676	2	IC,LINEAR,NE5532	U4,6
INTERFACE IC			
345-00751	2	IC,INTER,75492,LED DRVR	U2,3
345-02913	1	IC,INTER,NE594,DSP DRVR,8-SEG	U1
SS SW IC			
346-00770	1	IC,SS SWITCH,4053	U8

Lexicon Model 95 Front Panel #1 Board (continued)

PART NO.	QTY	DESCRIPTION	REF.
DSPLY/IND/LED			
430-01507	6	LED,DSPLY,5082-7613	DS1-6
430-01992	3	LED,RED,HE5082-4650	CR4,11,12
430-02013	4	LED,GRN,5082-4950	CR7-10
430-02014	2	LED,YEL,5082-4550	CR5,6
430-02285	3	LED,RED,.118 DIA	CR1-3
430-02902	3	LED,DSPLY,BAR,10 SEG	DS7-9
TOGGLE SWITCH			
450-01073	4	SW,TGL,1P2T,BLK BUSH,PC,GOLD C	SW1-4
SOCKETS			
520-00941	4	IC SCKT,8 PIN,PC,LO-PRO	U4-7
520-00942	2	IC SCKT,14 PIN,PC,LO-PRO	U2,3
520-00943	1	IC SCKT,16 PIN,PC,LO-PRO	U8
520-02177	1	IC SCKT,18 PIN,PC,LO-PRO	U1
520-02341	6	IC SCKT,14 PIN,WRAP-1L	DS1-6
520-02932	3	IC SCKT,20 PIN,WRAP-2L	DS7-9
INSUL/SPACRS			
630-02408	3	SPCR,#4CLX7/16,3/16RD,NYL	CR1-3 MTG
630-02409	9	SPCR,#6CLX5/8,1/4RD,NYL	CR4-12 MTG
SPCR,NON-INSUL			
635-00950	2	SPCR,6-32X1/2,1/4RD,BRASS/ZN	FRONT PANEL BD MTG
635-01453	8	SPCR,SWAGE,6-32X1/2,1/4RD,BR/N	FRONT PANEL BD MTG
635-03082	1	SPCR,SWAGE,6-32X9/16,1/4RD	SP BRACKET MTG
635-03083	2	SPCR,6-32X3/4,1/4HEX,W STUD	FRONT PANEL MTG
MACHINE SCREWS			
640-01710	1	SCRW,6-32X1/4,PNH,PH,ZN	FP BD #1 MTG,
640-02746	10	SCRW,2-M3X.5MMX.175L,PNH,PH,ZN	SP MTG
640-03713	10	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	SP BRKT MTG(1),FPB#1 MTG(9)
BULK WIRE			
670-02837	3	CABLE,FLEX-JUMP,19C,1.5X0.1	J1,2,4
CHASSIS/MECH			
700-02995	1	CHASSIS,INSERT,FP,M95	
BRACKETS			
701-03148	1	BRACKET,SLIDE POT,M95	

Lexicon Model 95 Front Panel #2 Board

PART NO.	QTY	DESCRIPTION	REF.
CARBON FLM RES			
202-00542	2	RES,CF,5%,1/4W,4.7K OHM	R3,6
METAL FLM RES			
203-01230	2	RES,MF,1%,1/8W,8.25K OHM	R2,4
203-01673	2	RES,MF,1%,1/8W,16.5K OHM	R1,5
PSH BUT SWITCH			
453-02690	6	SW,PBM,1P1T,SQ,BLU,PC	SW1-6
NUTS			
643-00000	6	NUT NUT,5/16" SUPPLIED WITH 200-02616, 200-02999,200-03000 ON FP #1	
WASHERS			
644-00000	18	WSHR WSHR,INT STAR SUPPLIED WITH 200-02616, 200-02999,200-03000 ON FP #1 (IF (THESE ARE NOT ALLEN-BRADLEY PARTS, QUANTITY IS REDUCED TO 6.00EA)	

Lexicon Model 95 Motherboard

PART NO.	QTY	DESCRIPTION	REF.
TRIM RESISTORS			
201-00159	1	RES,TRM,ST,PC,100K,SA,CER	R74
201-00427	1	RES,TRM,ST,PC,1K,SA,CER	R57
201-00430	1	RES,TRM,ST,PC,2K,SA,CER	R116
201-00439	7	RES,TRM,ST,PC,25K,SA,CER	R64,67,68,71-73,140
201-01619	1	RES,TRM,ST,PC,500 OHM,SA,CER	R70
CARBON FLM RES			
202-00506	2	RES,CF,5%,1/4W,20 OHM	R23,105
202-00510	1	RES,CF,5%,1/4W,51 OHM	R63
202-00514	11	RES,CF,5%,1/4W,100 OHM	R2,3,6,10,11,43,62,86,122,178,183
202-00518	1	RES,CF,5%,1/4W,220 OHM	R208
202-00519	1	RES,CF,5%,1/4W,240 OHM	R24
202-00525	1	RES,CF,5%,1/4W,510 OHM	R1
202-00529	8	RES,CF,5%,1/4W,1K OHM	R18,20-22,25,27,44,176
202-00531	9	RES,CF,5%,1/4W,1.5K OHM	R60,61,69,82-85,96,152
202-00540	1	RES,CF,5%,1/4W,3.9K OHM	R184
202-00542	6	RES,CF,5%,1/4W,4.7K OHM	R14,15,17,65,89,231
202-00543	2	RES,CF,5%,1/4W,5.1K OHM	R30,153
202-00544	1	RES,CF,5%,1/4W,5.6K OHM	R180
202-00549	20	RES,CF,5%,1/4W,10K OHM	R4,5,7-9,12,13,16,26,R49-52 R111-114,117,150,177
202-00555	7	RES,CF,5%,1/4W,20K OHM	R19,99,106,181,182,226,230
202-00564	5	RES,CF,5%,1/4W,51K OHM	R119,148,154,206,207
202-00570	7	RES,CF,5%,1/4W,100K OHM	R66,118,120,123,124,151,179
202-00580	1	RES,CF,5%,1/4W,1M OHM	R229
202-01228	3	RES,CF,5%,1/4W,620 OHM	R110,115,139
202-01497	2	RES,CF,5%,1/4W,2M OHM	R31,225
METAL FLM RES			
203-00450	2	RES,MF,1%,1/8W,100 OHM	R55,56
203-00454	2	RES,MF,1%,1/8W,357 OHM	R164,171
203-00456	1	RES,MF,1%,1/8W,1.00K OHM	R224
203-00459	4	RES,MF,1%,1/8W,2.00K OHM	R80,81,87,88
203-00460	1	RES,MF,1%,1/8W,2.15K OHM	R209
203-00461	1	RES,MF,1%,1/8W,2.43K OHM	R95
203-00462	1	RES,MF,1%,1/8W,2.55K OHM	R40
203-00464	35	RES,MF,1%,1/8W,4.99K OHM	R32-34,38,39,77-79,92,93,132, R133,137,138,149,159,161,165, R166,172,173,193,195,198,200, R203,205,212,213,216-218,221-223
203-00465	2	RES,MF,1%,1/8W,6.49K OHM	R156,228
203-00466	1	RES,MF,1%,1/8W,6.81K OHM	R185
203-00467	4	RES,MF,1%,1/8W,7.15K OHM	R35,90,196,201
203-00468	2	RES,MF,1%,1/8W,7.50K OHM	R127,142

Lexicon Model 95 Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
METAL FLM RES (continued)			
203-00470	1	RES,MF,1%,1/8W,9.53K OHM	R58
203-00471	16	RES,MF,1%,1/8W,10.0K OHM	R28,29,45,47,48,59,75,76,107, R108,144,146,147,155 (ECO QTY 2)
203-00476	1	RES,MF,1%,1/8W,12.1K OHM	R46
203-00482	6	RES,MF,1%,1/8W,20.0K OHM	R97,100,101,141,143,145
203-00487	1	RES,MF,1%,1/8W,30.1K OHM	R125
203-00489	1	RES,MF,1%,1/8W,71.5K OHM	R109
203-00491	2	RES,MF,1%,1/8W,100K OHM	R53,54
203-00493	1	RES,MF,1%,1/8W,215K OHM	R126
203-01137	1	RES,MF,1%,1/8W,4.12K OHM	R211
203-01139	1	RES,MF,1%,1/8W,21.5K OHM	R98
203-01145	2	RES,MF,1%,1/8W,1.24M OHM	R36,94
203-01246	6	RES,MF,1%,1/8W,17.4K OHM	R130,131,135,136,190,191
203-01489	1	RES,MF,1%,1/8W,499 OHM	R42
203-01490	1	RES,MF,1%,1/8W,3.09K OHM	R41
203-01491	2	RES,MF,1%,1/8W,4.22K OHM	R215,220
203-01492	2	RES,MF,1%,1/8W,7.68K OHM	R187,188
203-01663	2	RES,MF,1%,1/8W,34.0K OHM	R102,104
203-01996	1	RES,MF,1/2%,1/8W,3.01K OHM	R192
203-02010	2	RES,MF,1%,1/8W,4.87K OHM	R163,170
203-02290	2	RES,MF,1%,1/8W,1.21K OHM	R214,219
203-02291	3	RES,MF,1%,1/8W,5.49K OHM	R129,134,189
203-02353	2	RES,MF,1%,1/8W,49.9K OHM	R37,91
203-02397	2	RES,MF,1%,1/8W,158K OHM	R162,169
203-02610	2	RES,MF,1%,1/8W,1.65K OHM	R197,202
203-02611	1	RES,MF,1%,1/8W,5.62K OHM	R160
203-02651	1	RES,MF,1%,1/8W,4.02K OHM	R194
203-02652	1	RES,MF,1%,1/8W,4.75K OHM	R157
203-02653	2	RES,MF,1%,1/8W,5.11K OHM	R199,204
203-02654	2	RES,MF,1%,1/8W,5.90K OHM	R168,175
203-02655	1	RES,MF,1%,1/8W,6.04K OHM	R210
203-02656	2	RES,MF,1%,1/8W,182K OHM	R167,174
203-02657	1	RES,MF,1%,1/8W,221K OHM	R128
203-02659	1	RES,MF,1%,1/8W,604 OHM	R158
203-02660	1	RES,MF,1%,1/8W,3.57K OHM	R186
203-02673	1	RES,MF,1%,PTC,500 OHM	R103
203-02702	2	RES,MF,1%,1/8W,8.66K OHM	R121,227
NETWORK RES			
205-00240	3	RES,NET,SIP,2%,3.3KX7	RP2,5,7
205-00241	1	RES,NET,SIP,2%,4.7KX7	RP6
205-01133	2	RES,NET,DIP,1%,10KX8	RP8,9
205-01155	3	RES,NET,DIP,2%,68X7	RP1,3,4
205-01456	1	RES,NET,DIP,0.5%/0.1%,1KX8	RP10

Lexicon Model 95 Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
ELECTROLYT CAP			
240-00611	5	CAP,ELEC,22uF,16V,RAD	C101,127,129,165,166
240-00613	6	CAP,ELEC,22uF,25V,RAD	C6,12,13,98-100
240-00614	7	CAP,ELEC,47uF,16V,RAD	C32,50,59,130,137,187,197
240-02251	1	CAP,ELEC,10,000uF,16V,10,AX	C7
240-03338	2	CAP,ELEC,2200uF,35V,RAD	C10,11
TANTALUM CAP			
241-00651	2	CAP,TANT,.22uF,35V,RAD	C185,254
241-02589	3	CAP,TANT,4.7uF,25V,5%,RAD	C93,114,131
PCRB/PP CAP			
244-00660	1	CAP,MYL,.01uF,100V,10%,RAD	C85
244-01166	4	CAP,PP,240pF,2.5%	C112,113,164,188
244-01167	2	CAP,PP,750pF,2.5%	C78,79
244-01169	53	CAP,PP,2200pF,2.5%	C138,139,141,142,144-146,149-153, C156,157,167,168,171-174,177-180, C183,184,189,190,199,200,203,204, C207,208,211-214,217,218,229-231, C234,235,238,239,242-245,248,249
244-01488	1	CAP,MYL,.22uF,100V,10%,RAD	C122
244-02104	6	CAP,PP,100pF,160V,2.5%,AX	C223-228
CERAMIC CAP			
245-00586	2	CAP,CER,30pF,50V,10%	C57,117
245-00590	18	CAP,CER,150pF,50V,10%	C16,17,39,87,91,92,123,125,126, C132,158,159,191-194,219,220
245-00593	1	CAP,CER,560pF,50V,10%,Z5F	C55
245-00594	2	CAP,CER,.001uF,500V,10%,Z5F	C106,107
245-00596	2	CAP,CER,.005uF,1.6KV,Z5U	C1,2
245-00600	67	CAP,CER,.02uF,35V,80/20%	C3,5,8,9,14,15,18,19,33-38,40-49, C51-54,56,58,60,61,63-77,80,81, C94,97,102,103,110,111,118,119, C124,128,160,163,195,196,221,222, C252,253
245-00607	1	CAP,CER,39pF,50V,10%	C105
245-01164	32	CAP,CER,10pF,50V,10%	C121,133-136,140,147,148,154,155, C161,162,169,170,175,176,181,182, C186,198,201,202,209,210,215,216, C232,233,240,241,246,247
245-01651	33	CAP,CER,.1uF,50V,80/20%	C4,20-31,62,82-84,86,88-90,96, C104,116,120,143,205,206,236, C237,250,251,255
245-02105	2	CAP,CER,5pF,500V,10%,NPO	C95,115
INDUCTORS			
270-00779	4	FERRITE,BEAD	FB1-4

Lexicon Model 95 Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
DIODES			
300-01026	1	DIODE,1N753	CR1
300-01029	24	DIODE,1N914 AND 4148	CR14,15,18,19,26-28,35,36, CR42-47,53-61
300-01030	8	DIODE,1N4004 AND 4005	CR6-9,16,17,24,25
300-01032	8	DIODE,1N5404	CR2-5,10-13
300-02401	12	DIODE,BAR 35,SCHOTTKY,LOW VF	CR20,21,29-32,37-40,48,51
300-02672	2	DIODE,VARACTOR,A.M.TUNING	CR33,34
TRANSISTORS			
310-01003	3	TRANSISTOR,MPS2369	Q4-6
310-01007	3	TRANSISTOR,2N3904	Q2,7,8
310-01008	1	TRANSISTOR,2N3906	Q3
DIGITAL/CMOS IC			
330-00692	5	IC,DIGITAL,74LS00	U20,22,42,48,49
330-00693	1	IC,DIGITAL,74LS02	U59
330-00695	3	IC,DIGITAL,74LS04	U31,44,67
330-00698	1	IC,DIGITAL,74LS14	U47
330-00703	3	IC,DIGITAL,74LS74	U32,33,41
330-00708	1	IC,DIGITAL,74LS107	U46
330-00711	2	IC,DIGITAL,74LS157	U15,16
330-00712	1	IC,DIGITAL,74LS163	U17
330-00716	3	IC,DIGITAL,74LS283	U12-14
330-00718	4	IC,DIGITAL,74LS367	U50,51,60,61
330-01283	2	IC,DIGITAL,74LS139	U21,57
330-01291	3	IC,DIGITAL,74LS273	U52-54
330-01293	8	IC,DIGITAL,74LS374	U23-28,34,35
330-01294	1	IC,DIGITAL,74LS377	U30
330-01295	3	IC,DIGITAL,74LS393	U18,19,39
330-01313	1	IC,DIGITAL,74LS86	U40
330-01573	2	IC,DIGITAL,74LS32	U56,58
330-02085	1	IC,DIGITAL,AM25L04	U43
LINEAR IC			
340-00725	1	IC,LINEAR,LM311	U78
340-00733	1	IC,LINEAR,CA 3039	U70
340-00735	1	IC,LINEAR,CA 3080AE	U79
340-00740	3	IC,LINEAR,4558	U4,5,68
340-00744	1	IC,LINEAR,78L05	U86
340-01183	1	IC,LINEAR,LF 356	U63
340-01566	15	IC,LINEAR,LF353,DUAL OP AMP	U73,77,80,82,83,91-94,104-106
340-02086	1	IC,LINEAR,LM317LH,TO-39	U71
340-02396	4	IC,LINEAR,HA 2515-5	U62,64,75,76
340-02674	1	IC,LINEAR,CMP-05FZ	U65
340-02676	9	IC,LINEAR,NE5532	U72,81,85,87,88,90,102,103,107 U109-111

Lexicon Model 95 Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
SS SW IC			
346-01366	2	IC,SS,SWITCH,4016	U69,74
346-02677	7	IC,SS SWITCH,DG211	U95-101
MEMORY IC			
350-01820	2	IC,RAM,2114	U36,37
350-02640	1	IC,ROM,82S123,M95	U29
350-02689	6	IC,DRAM,4164,64KX1,250NS	U6-11
CONVERTER IC			
355-02087	1	DAC,AM6012DC	U66
355-02903	1	IC,CONVERTER,ADC 0809	U55
MICROPROC IC			
365-02530	1	IC,uPROC,MK3880N-4,Z-80A CPU	U45
OPTO ISLTOR IC			
375-02829	3	IC,OPTO-ISOLATOR,CLM50	U84,89,108
CRYSTALS			
390-01642	1	CRYSTAL,4.9152 MHz	Y1
SLIDE SWITCH			
451-02230	1	SW,SL,2P2T,V-CHNG,PC,4A	SW2
PSH BUT SWITCH			
453-02111	2	SW,PBPP,2P2T,SCHADOW,PCRA	SW3,4
453-02226	1	SW,PBPP,2P2T,LINE RATED,PCRA	SW1
TRANSFORMERS			
470-00037	1	XFORMER,4.4MHz	T2

Lexicon Model 95 Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
PC MNT CONN			
510-01514	1	CONN,POST,100X025,HDR,8MC	P3
510-02106	9	1/4" PHONE JACK,PCRA,3C,SWITCH	J2-6,8-11
510-02534	1	CONN,XLR,3MC,PCRA	J7
510-02535	1	CONN,XLR,3FC,PCRA	J12
SOCKETS			
520-00941	37	IC SCKT,8 PIN,PC,LO-PRO	U4,5,62-64,68,72,73,75-85 U87-94,102-111
520-00942	22	IC SCKT,14 PIN,PC,LO-PRO	U18-20,22,31-33,39-42,44 U46-49,56,58,59,67,69,74
520-00943	26	IC SCKT,16 PIN,PC,LO-PRO	U6-17,21,29,50,51,57,60,61,U95-101
520-00945	2	IC SCKT,24 PIN,PC,LO-PRO	U38,43
520-00946	1	IC SCKT,40 PIN,PC,LO-PRO	U45
520-01361	13	IC SCKT,20 PIN,PC,LO-PRO	U23-28,30,34,35,52-54,66
520-01458	1	IC SCKT,28 PIN,PC,LO-PRO	U55
520-02177	2	IC SCKT,18 PIN,PC,LO-PRO	U36,37
INSUL/SPACRS			
630-01894	1	INSUL,SEMI,TO-5 SPCR	U71
MACHINE SCREWS			
640-01841	2	SCRW,2-56X1/4,PNH,PH,ZN	SW1 MTG
640-02715	4	SCRW,4-40X1/4,FH,PH,ZN	J7,12 MTG
THRD-FORM SCRW			
641-01703	2	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	J7,12
NUTS			
643-01855	2	NUT,2-56,HEX,SMALL,ZN	SW1 BRKT
WASHERS			
644-01854	2	WSHR,LOCK,SPLIT,#2	SW1 MTG

Lexicon Model 95 Mechanical Parts List

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-02991	1	MANUAL,OWNER'S,M95	
SCR			
320-01014	1	TRANSISTOR,C122F1,SCR	Q1
LINEAR IC			
340-00742	1	IC,LINEAR,7805 (LM 340 T-5)	U1
340-00745	1	IC,LINEAR,7815 (LM 340 T-15)	U2
340-00747	1	IC,LINEAR,7915 (LM 320 T-15)	U3
MEMORY IC			
350-04043	1	IC,ROM,2732,M95,V1.0	U38
CABLE CONN			
490-00396	1	CONN,AC AND RFI FILTER	J1
STRAIN REL			
530-02489	2	TIE,CABLE,NYL,.1"X4"	T1
GROMMETS			
540-03003	1	GUARD,DUST,M95	FRONT PANEL
FEET			
541-00780	4	BUMPER,FEET,3-M #SJ5023	BOTTOM COVER
KNOBS/CAPS			
550-02228	2	BUTTON,TANG,WHT/BLK	SW3,4
550-02229	1	BUTTON,TANG,WHT/RED	SW1
550-02344	2	KNOB,21MM,1/8SHFT,BLK	R1,2
550-02627	10	KNOB,SLIDE,TANG,BLK/WHT LN	R8-12,33-37
550-02695	2	KNOB CAP,21MM,BLU	R1,2
550-03004	4	KNOB,11MM,118SHFT,BLK/WHT LN	R4-7
550-03005	4	KNOB CAP,11MM,BLU/WHT LN	R4-7
PC HDWR			
610-02269	3	HARDWARE,PC,RICHCO #MB-3-156	FISH PAPER MTG
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,#6,.020THK	GRND LUG

Lexicon Model 95 Mechanical Parts List (continued)

PART NO.	QTY	DESCRIPTION	REF.
INSUL/SPACRS			
630-00952	4	INSUL,SEMI,BUSHING,TO-220	Q1,U1-3 MTG
630-01853	4	INSUL,SEMI,SIL RUB,TO-220	Q1,U1-3 MTG
630-02267	1	SPCR,PCB PUSHON/STUD,1/4	SW1
630-02529	1	SPCR,#8CLX10,1/4RD,PHEN	SW1
630-02705	6	WSHR,FL,#6CLX1/40DX.02,BLK,NYL	FRONT PANEL MTG
MACHINE SCREWS			
640-01706	6	SCRW,4-40X3/8,PNH,PH,ZN	Q1,U1-3 MTG,J1 MTG(2)
640-01713	1	SCRW,6-32X5/16,PNH,PH,ZN	GRND LUG MTG
640-01721	2	SCRW,8-32X3/8,PNH,PH,ZN	T1 MTG
640-02706	6	SCRW,6-32X1/4,BH,SCKT,BLK	FRONT PANEL MTG
640-02749	20	SCRW,6-32X1/4,PNH,PH,SEMS,BLK	T&B COVER MTG
640-03713	10	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	CHASSIS INSERT MTG(4)
NUTS			
643-00000	9	NUT	J2-6,8-11 MTG NUT,3/8-24X1/2 SUPPLIED WITH 510-02106 ON MTHBD
643-01729	1	NUT,6-32,HEX,SMALL,ZN	GRND LUG MTG
643-01732	2	NUT,4-40,KEP,ZN	J1 MTG
643-01733	4	NUT,4-40,HEX,SMALL,ZN	Q1,U1-3 MTG
643-01734	2	NUT,8-32,KEP,ZN	T1 MTG
WASHERS			
644-00000	9	WSHR	J2-6,8-11 MTG WSHR,FLAT, .375IDX.615ODX.020 SUPPLIED WITH 510-02106 ON MTHBD
644-01736	4	WSHR,FL,#4CLX.218ODX.032THK	Q1,U1-3 MTG
644-01737	4	WSHR,LOCK,SPLIT,#4	Q1,U1-3 MTG
644-01738	9	WSHR,INT STAR,3/8CLX.690DX.031	J1-6,8-11 MTG
PRE-CUT WIRE			
675-02843	1	WIRE,18G,WHT,4",ST&T1/4X1/4	J1 WIRING
675-02847	1	WIRE,18G,BLK,4",ST&T1/4X1/4	J1 WIRING
675-02852	1	WIRE,16G,GRN,4",ST1/4XST&T1/4	J1 WIRING
CABLES/CORDS			
680-00841	1	CORD,POWER,PHILLIP #13E37-1	
CHASSIS/MECH			
700-02994	1	CHASSIS,WRAPAROUND,M95	
700-02998	2	COVER,TOP/BOTTOM,M95	

Lexicon Mo[redacted]echanical Parts List (continued)

PART NO.	QTY	DESCRIPTION	REF.
PANELS			
702-02996	1	PANEL,FRONT,M95	
702-02997	1	COVER,PROTECTIVE,M95	
LENS/PLATE/PANL			
703-02588	1	LENS,DISPLAY,M97	FRONT PANEL

Lexicon Model 95 Japan Fuse/Transformer Option

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01177	1	FUSE,3AG,FAST,.750AMP,115V	F1 -- MOTHERBOARD
440-01877	2	FUSE,5X20MM,SLO-BLO,1.25AMP	F3,4 -- MOTHERBOARD
440-02665	1	FUSE,5X20MM,SLO-BLO,3AMP,250V	F2 -- MOTHERBOARD
TRANSFORMERS			
470-01243	1	XFORMER,POWER,M93(JAPAN)	T1
ELECTRONIC HDWR			
600-00871	2	FUSE CLIP,1/4",PC	F1 -- MOTHERBOARD
600-02227	6	FUSE CLIP,20MM,PC	F2-4 -- MOTHERBOARD

Lexicon Model 95 North American Fuse/Transformer Option

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01177	1	FUSE,3AG,FAST,.750AMP,115V	F1 -- MOTHERBOARD
TRANSFORMERS			
470-00778	1	XFORMER,POWER,M93	T1
ELECTRONIC HDWR			
600-00871	2	FUSE CLIP,1/4",PC	F1 -- MOTHERBOARD

Lexicon Model 95 European Fuse/Transformer Option

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01877	2	FUSE,5X20MM,SLO-BLO,1.25AMP	F3,4 -- MOTHERBOARD
440-02665	1	FUSE,5X20MM,SLO-BLO,3AMP,250V	F2 -- MOTHERBOARD
440-03172	1	FUSE,5X20MM,SLO-BLO,.400AMP	F1 -- MOTHERBOARD
TRANSFORMERS			
470-00778	1	XFORMER,POWER,M93	T1
ELECTRONIC HDWR			
600-02227	8	FUSE CLIP,20MM,PC	F1-4

Lexicon Model 95 Memory Extension Option #1

PART NO.	QTY	DESCRIPTION	REF.
CERAMIC CAP			
245-01651	18	CAP,CER,.1uF,50V,80/20%	C1-18
MEMORY IC			
350-02689	6	IC,DRAM,4164,64KX1,250NS	U1-3,10-12
PC MNT CONN			
510-01070	2	CONN,POST,100X025,HDR,RA,18MC	P13
SOCKETS			
520-00943	18	IC SCKT,16 PIN,PC,LO-PRO	U1-18
MACHINE SCREWS			
640-01701	4	SCRW,4-40X1/4,PNH,PH,ZN	MTG BRKT TO MEM BD, MTG BRKT TO MTHBD
NUTS			
643-01732	2	NUT,4-40,KEP,ZN	MTG BRKT TO MEM BD
WASHERS			
644-01747	2	WSHR,INT STAR,#4	MTG BRKT TO MTHBD
CHASSIS/MECH			
700-00163	2	BRACKET,KEYSTONE #612	

Lexicon Model 95 Memory Extension Option #2

PART NO.	QTY	DESCRIPTION	REF.
CERAMIC CAP			
245-01651	18	CAP,CER,.1uF,50V,80/20%	C1-18
MEMORY IC			
350-02689	18	IC,DRAM,4164,64KX1,250NS	U1-18
PC MNT CONN			
510-01070	2	CONN,POST,100X025,HDR,RA,18MC	P13
SOCKETS			
520-00943	18	IC SCKT,16 PIN,PC,LO-PRO	U1-18
MACHINE SCREWS			
640-01701	4	SCRW,4-40X1/4,PNH,PH,ZN	MTG BRKT TO MEM BD, MTG BRKT TO MTHBD
NUTS			
643-01732	2	NUT,4-40,KEP,ZN	MTG BRKT TO MEM BD
WASHERS			
644-01747	2	WSHR,INT STAR,#4	MTG BRKT TO MTHBD
CHASSIS/MECH			
700-00163	2	BRACKET,KEYSTONE #612	

Lexicon Model 95 Retrofit -- Memory Extension Option #1

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-03684	1	INSTR,RETROFIT,MEM OPTIONS,M95	
CERAMIC CAP			
245-01651	18	CAP,CER,.1uF,50V,80/20%	C1-18
MEMORY IC			
350-02689	6	IC,DRAM,4164,64KX1,250NS	U1-3,10-12
PC MNT CONN			
510-01070	2	CONN,POST,100X025,HDR,RA,18MC	P13
SOCKETS			
520-00943	18	IC SCKT,16 PIN,PC,LO-PRO	U1-18
MACHINE SCREWS			
640-01701	6	SCRW,4-40X1/4,PNH,PH,ZN	MTG BRKT TO MEM BD (2), MTG BRKT TO MTHBD (2)
NUTS			
643-01732	2	NUT,4-40,KEP,ZN	MTG BRKT TO MEM BD
WASHERS			
644-01747	4	WSHR,INT STAR,#4	MTG BRKT TO MTHBD (2)
CHASSIS/MECH			
700-00163	2	BRACKET,KEYSTONE #612	

Lexicon Model 95 Retrofit -- Memory Extension Option #2

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-03684	1	INSTR,RETROFIT,MEM OPTIONS,M95	
CERAMIC CAP			
245-01651	18	CAP,CER,.1uF,50V,80/20%	C1-18
MEMORY IC			
350-02689	18	IC,DRAM,4164,64KX1,250NS	U1-18
PC MNT CONN			
510-01070	2	CONN,POST,100X025,HDR,RA,18MC	P13
SOCKETS			
520-00943	18	IC SCKT,16 PIN,PC,LO-PRO	U1-18
MACHINE SCREWS			
640-01701	6	SCRW,4-40X1/4,PNH,PH,ZN	MTG BRKT TO MEM BD (2) MTG BRKT TO MTHBD (2)
NUTS			
643-01732	2	NUT,4-40,KEP,ZN	MTG BRKT TO MEM BD
WASHERS			
644-01747	4	WSHR,INT STAR,#4	MTG BRKT TO MTHBD (2)
CHASSIS/MECH			
700-00163	2	BRACKET,KEYSTONE #612	

Lexicon Model 95 Retrofit -- Memory Extension Option #1 TO #2

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-03684	1	INSTR,RETROFIT,MEM OPTIONS,M95	
MEMORY IC			
350-02689	12	IC,DRAM,4164,64KX1,250NS	

6 Schematics and assembly drawings

The following schematics and assembly drawings are contained in this section in the order listed:

Schematics

1. Motherboard, Analog In
2. Motherboard, Analog Out
3. Motherboard, Converter
4. Motherboard, VCO
5. Motherboard, CPU
6. Motherboard, Delay
7. Motherboard, Power Supply
8. Memory Extension Option
9. Front Panel Board, Audio
10. Front Panel Board, Digital

Assembly Drawings

1. Motherboard
2. Memory Extension Option
3. Front Panel #1
4. Front Panel #2
5. Front Panel Detail

7 ECOs

ECO #: 821230-00

Date Effective: 12/30/82

Purpose of Change: To ease calibration problems of the balanced Master Output buffer.

Change	Qty	Part #	Description	Reference
Delete:	2	245-00590	CAP,CER,150pF,500V,10%	C106,107
	2	245-01164	CAP,CER,10pF	C108,109
Add:	2	245-00594	CAP,CER,.001uF,500V,10%Z5F	C106,107

ECO #: 830111-00

Date Effective: 01/11/83

Purpose of Change: To flatten frequency response in passband.

Change	Qty	Part #	Description	Reference
Delete:	1	203-00492	RES,MF,1%,1/8W,200K OHM	R126
	2	203-01136	RES,MF,1%,1/8W,5.76K OHM	R156,228
Add:	1	203-00493	RES,MF,1%,1/8W,215K OHM	R126
	2	203-00465	RES,MF,1%,1/8W,6.49K OHM	R156,228

ECO #: 830210-00

Date Effective: 02/10/83

Purpose of Change: To ensure that +12 dB level LED will turn on near its its intended level, despite worst case supply voltages.

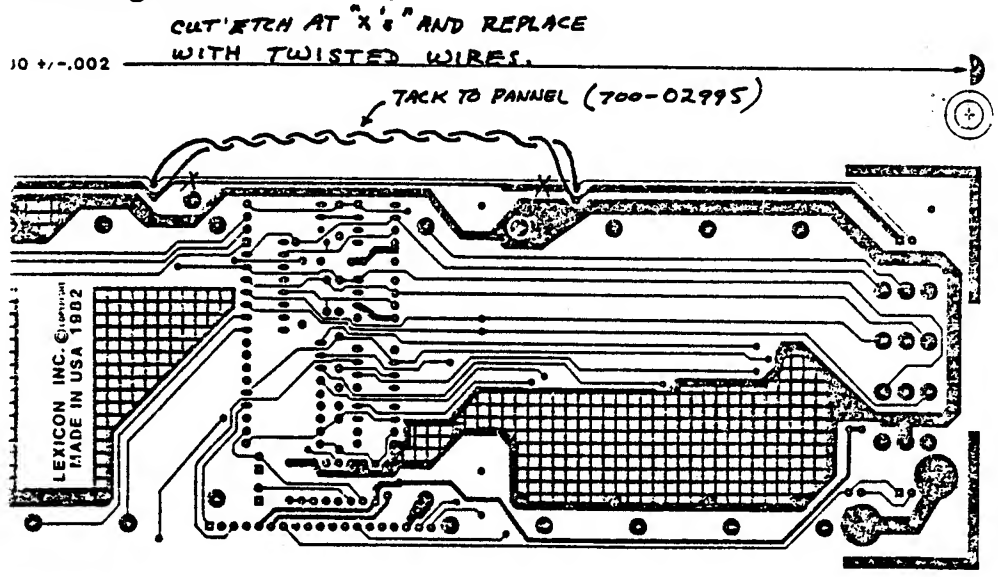
Change	Qty	Part #	Description	Reference
Delete:	1	202-00549	RES,CF,5%,1/4W,10K OHM	R121
	1	202-01225	RES,CF,5%,1/4W,6.2K OHM	R149
Add:	1	203-02702	RES,MF,1%,1/8W,8.66K OHM	R121
	1	203-00464	RES,MF,1%,1/8W,4.99K OHM	R149

ECO #: 830317-00

Date Effective: 03/17/83

Purpose of Change: To reduce switching circuit noise from analog circuits.

Change: Cut Etch and replace with loose twisted pair, tacked with silicone to inside surface of metal basket behind front panel PCB. See drawing below.



ECO #: 830408-00

Date Effective: 04/08/83

Purpose of Change: To improve accuracy of displayed delay times in VCO mode.

Change	Qty	Part #	Description	Reference
Delete:	1	202-00549	RES,CF,5%,1/4W,10K OHM	R28,29
	1	202-00570	RES,CF,5%,1/4W,100K OHM	R53,54
Add:	1	203-00471	RES,MF,1%,1/8W,10.0K OHM	R28,29
	1	203-00491	RES,MF,1%,1/8W,100K OHM	R53,54

ECO #: 830429-00

Date Effective: 04/29/83

Purpose of Change: To ensure that VCO reaches high end of range.

Change	Qty	Part #	Description	Reference
Delete:	1	245-00588	CAP,CER,100pF,1000V,10%	C105
Add:	1	245-00607	CAP,CER,39pF,1000V,10%	C105

ECO #: 830517-01

Date Effective: 05/17/83

Purpose of Change: To correct distortion problems at certain delay settings or elevated temperature.

Change	Qty	Part #	Description	Reference
Delete:	1	245-02105	CAP,CER,5pF,500V,10%,NPO	C117
Add:	1	245-00586	CAP,CER,30pF,100V,10%	C117

ECO #: 830517-02

Date Effective: 05/17/83

Purpose of Change: Ease calibration of balanced output stage

Change	Qty	Part #	Description	Reference
Delete:	1	203-00471	RES,MF,1%,1/8W,10.0K OHM	R76
	1	202-00514	RES,CF,5%,1/4W,100 OHM	R55,56
Add:	1	203-00472	RES,MF,1%,1/8W,10.2K OHM	R76
Add:	1	203-00450	RES,MF,1%,1/8W,100 OHM	R55,56

ECO #: 840710-00

Date Effective: 07/10/84

Purpose of Change: Ease calibration of balanced output stage

Change	Qty	Part #	Description	Reference
Delete:	1	203-00472	RES,MF,1%,1/8W,10.2K OHM	R76
Add:	1	203-00471	RES,MF,1%,1/8W,10.0K OHM	R76
Add:	1	203-00471	RES,MF,1%,1/8W,10.0K OHM	*

*This resistor must be added to the bottom of the motherboard (circuit side) as shown below: